FIG. 1

(Related Art)

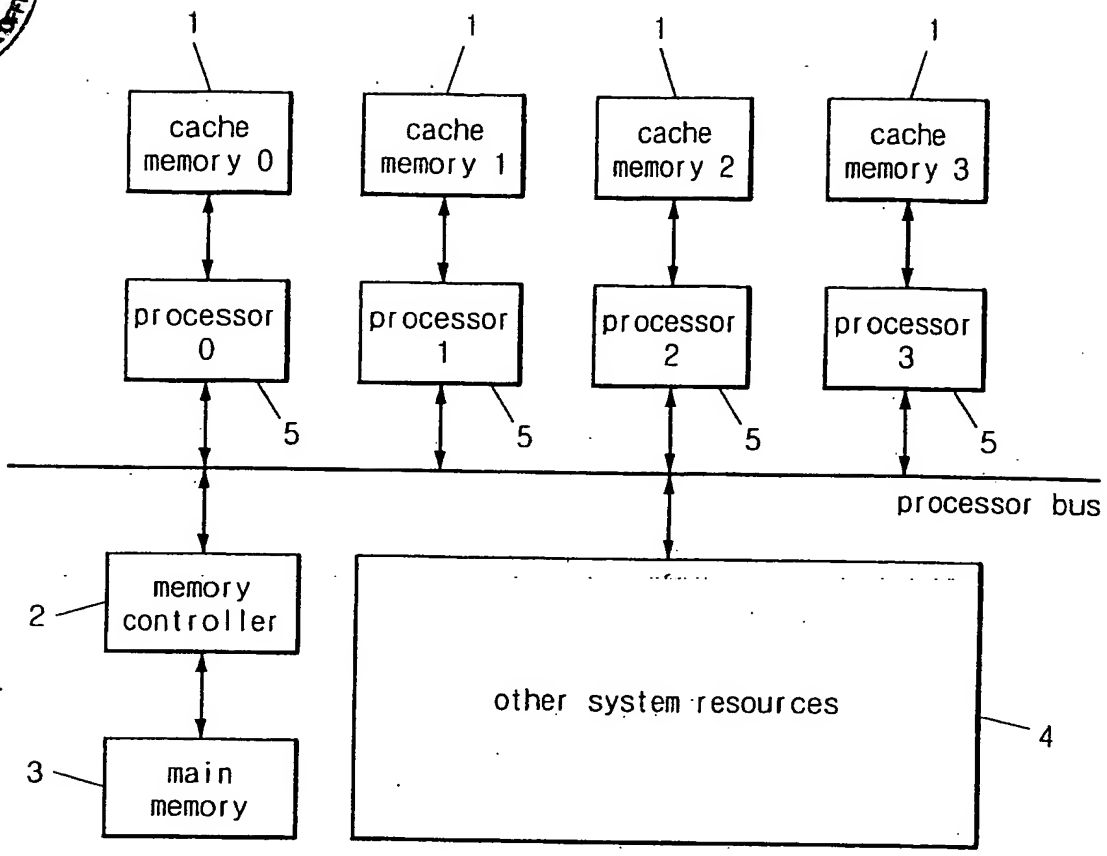


FIG. 2

(Related Art)

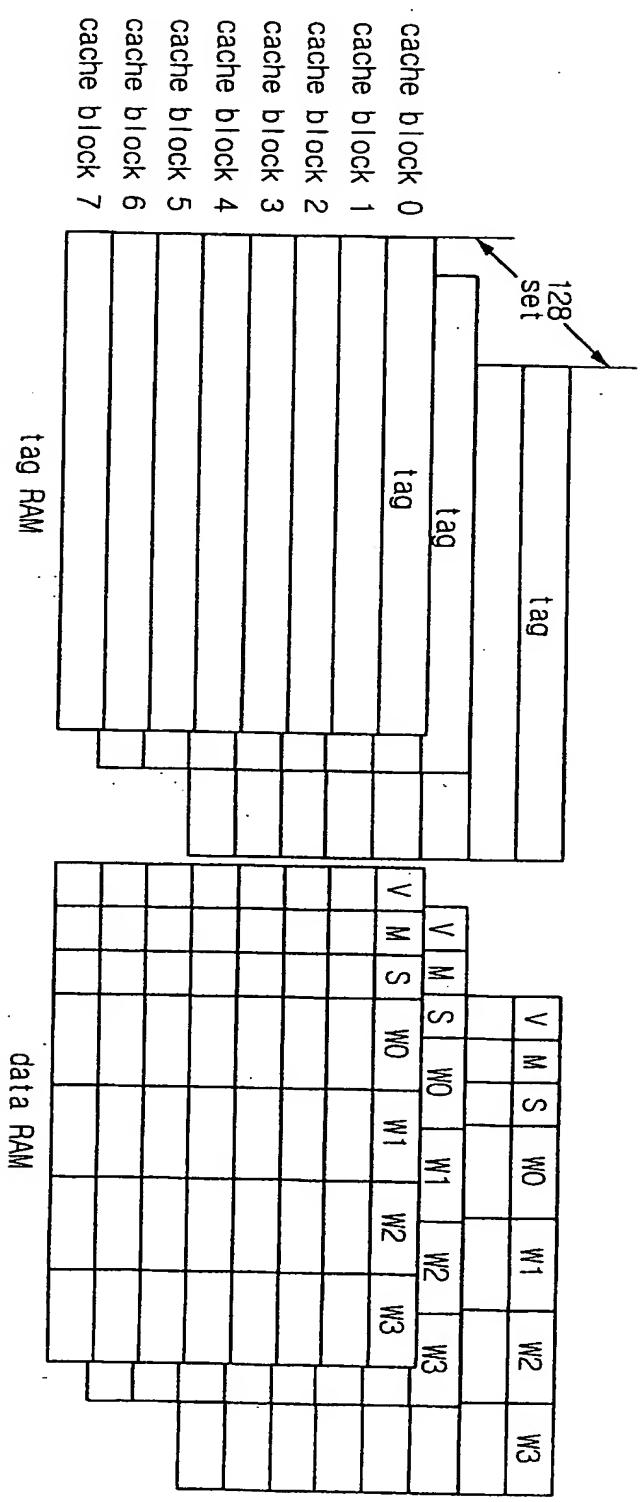


FIG. 3

(Related Art)

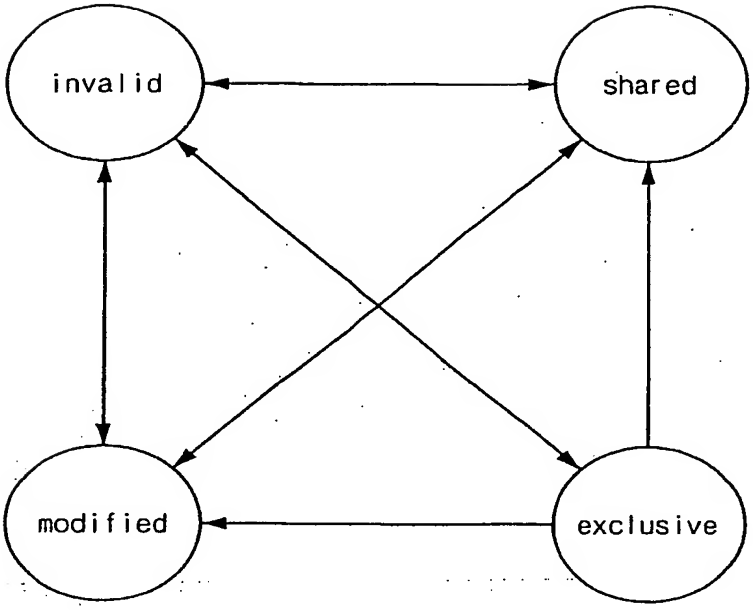


FIG. 4

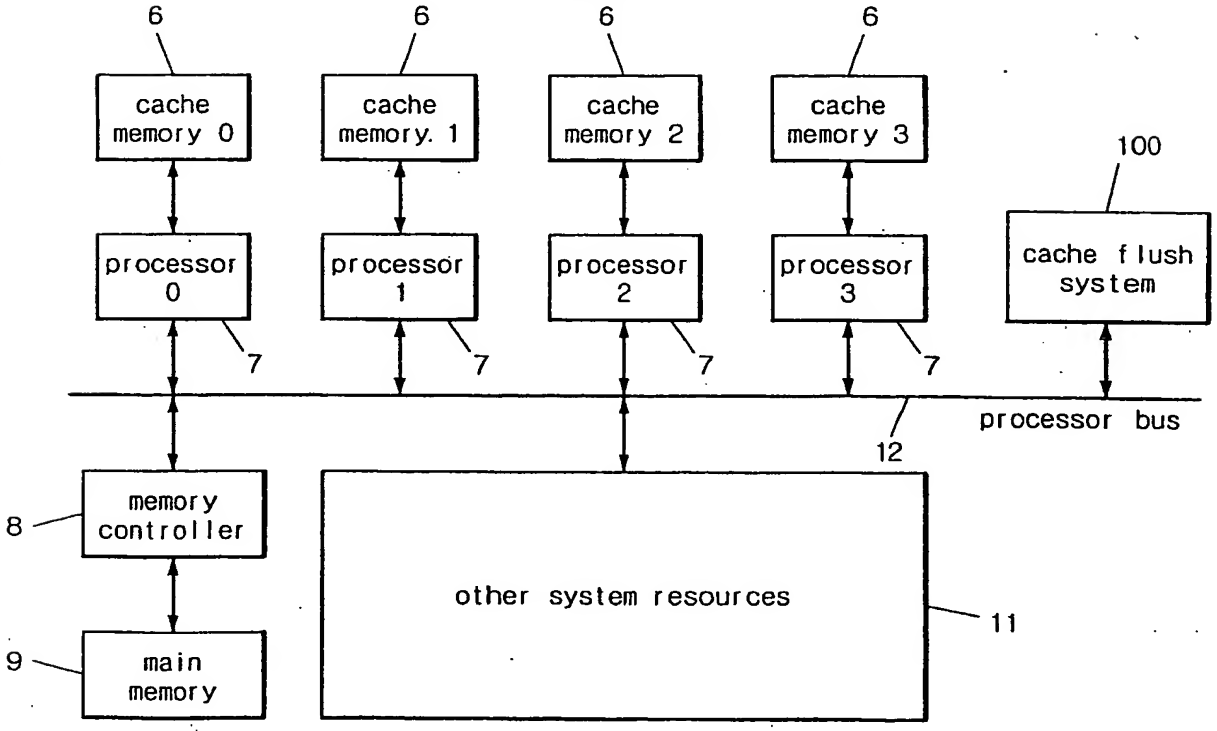


FIG. 5

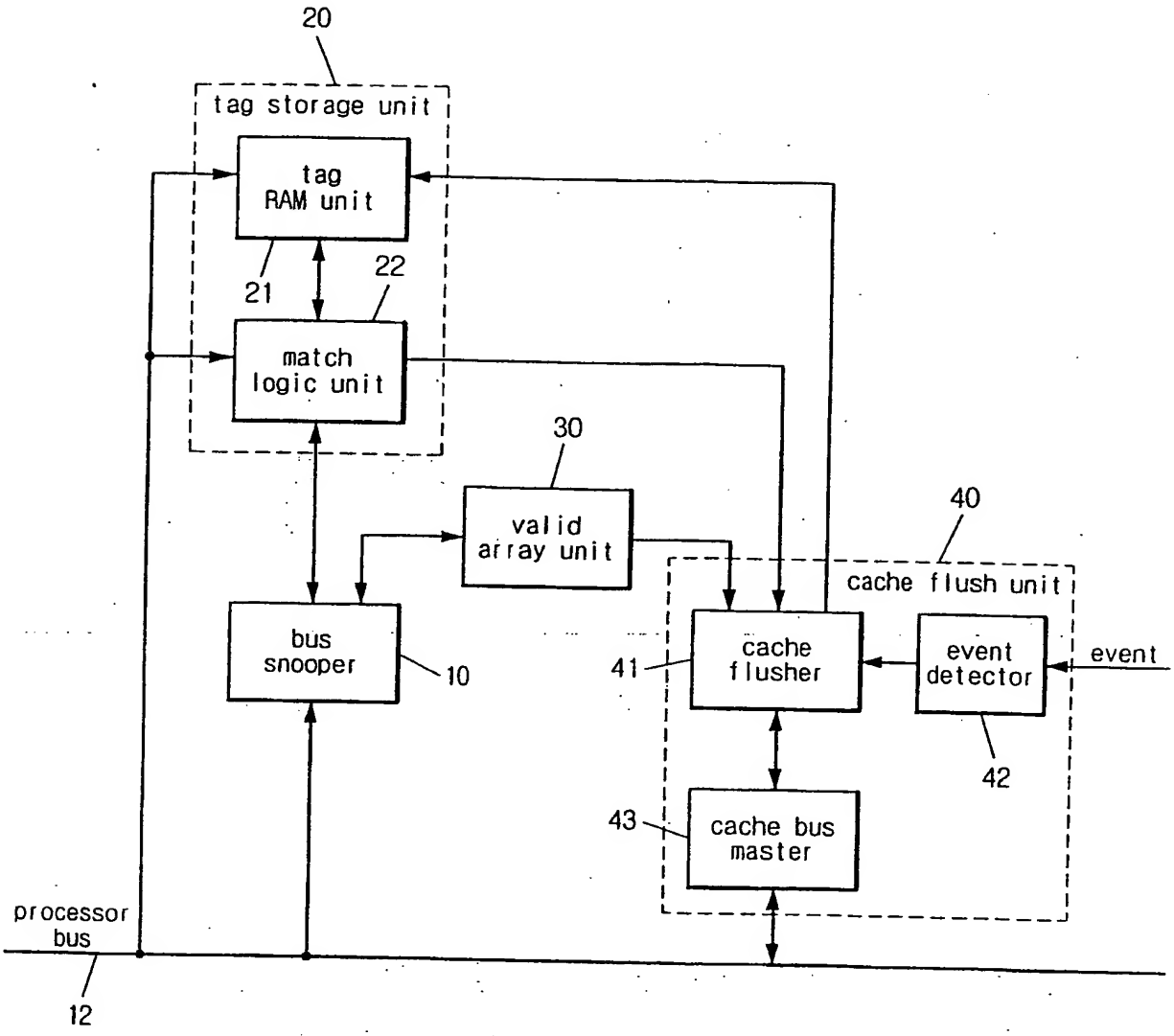

20
tag storage unit
tag
RAM unit
21
22
match
logic unit
30
valid
array unit
40
cache flush unit
bus
snooper
10
41
cache
flusher
event
detector
event
42
43
cache bus
master
processor
bus
12

FIG. 6a

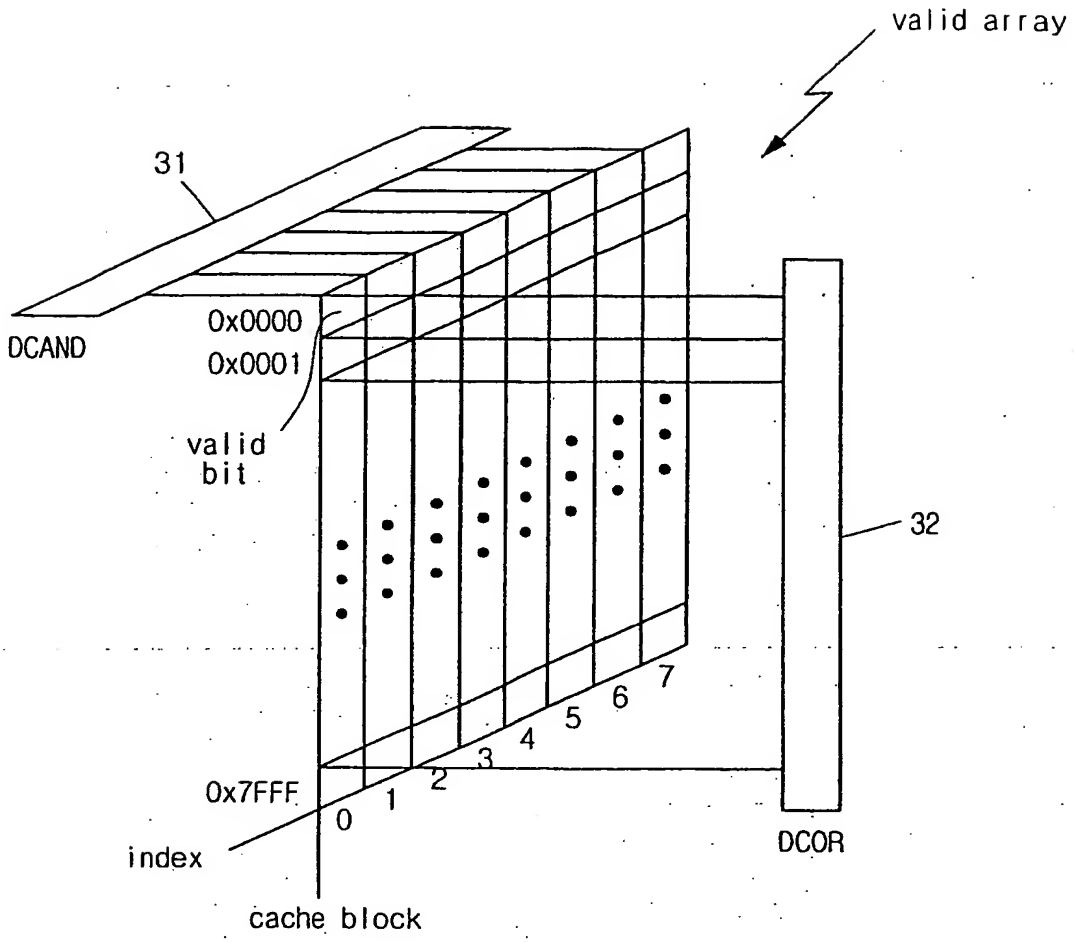

valid array
31
DCAND
0x0000
0x0001
valid
bit
32
0
1
2
3
4
5
6
7
0x7FFF
index
cache block
DCOR

FIG. 6b

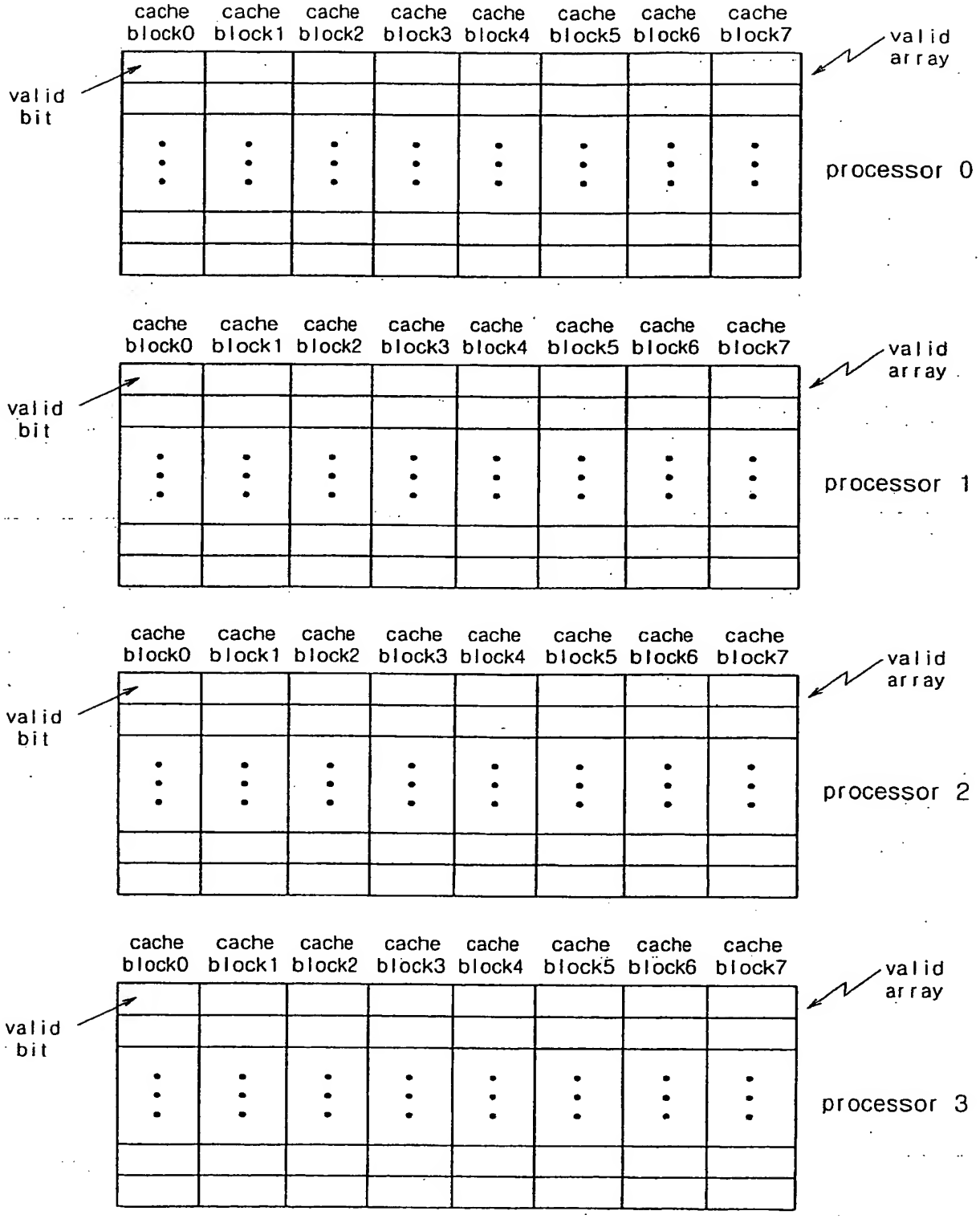

cache block0
cache block1
cache block2
cache block3
cache block4
cache block5
cache block6
cache block7
valid bit
valid array
processor 0
processor 1
processor 2
processor 3

FIG. 7

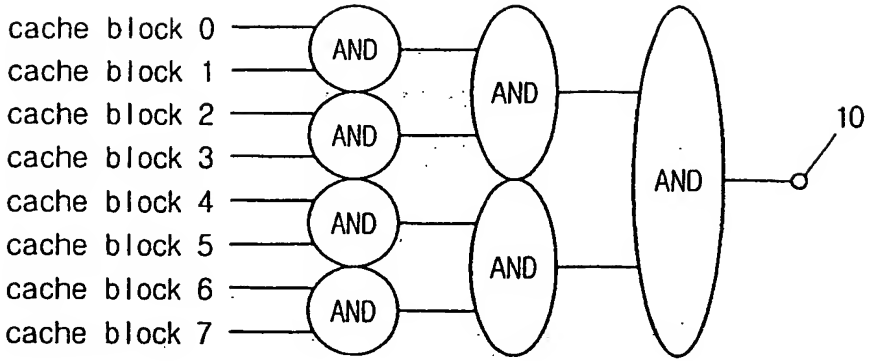

cache block 0
cache block 1
cache block 2
cache block 3
cache block 4
cache block 5
cache block 6
cache block 7
AND
AND
AND
AND
AND
AND
AND
10

FIG. 8

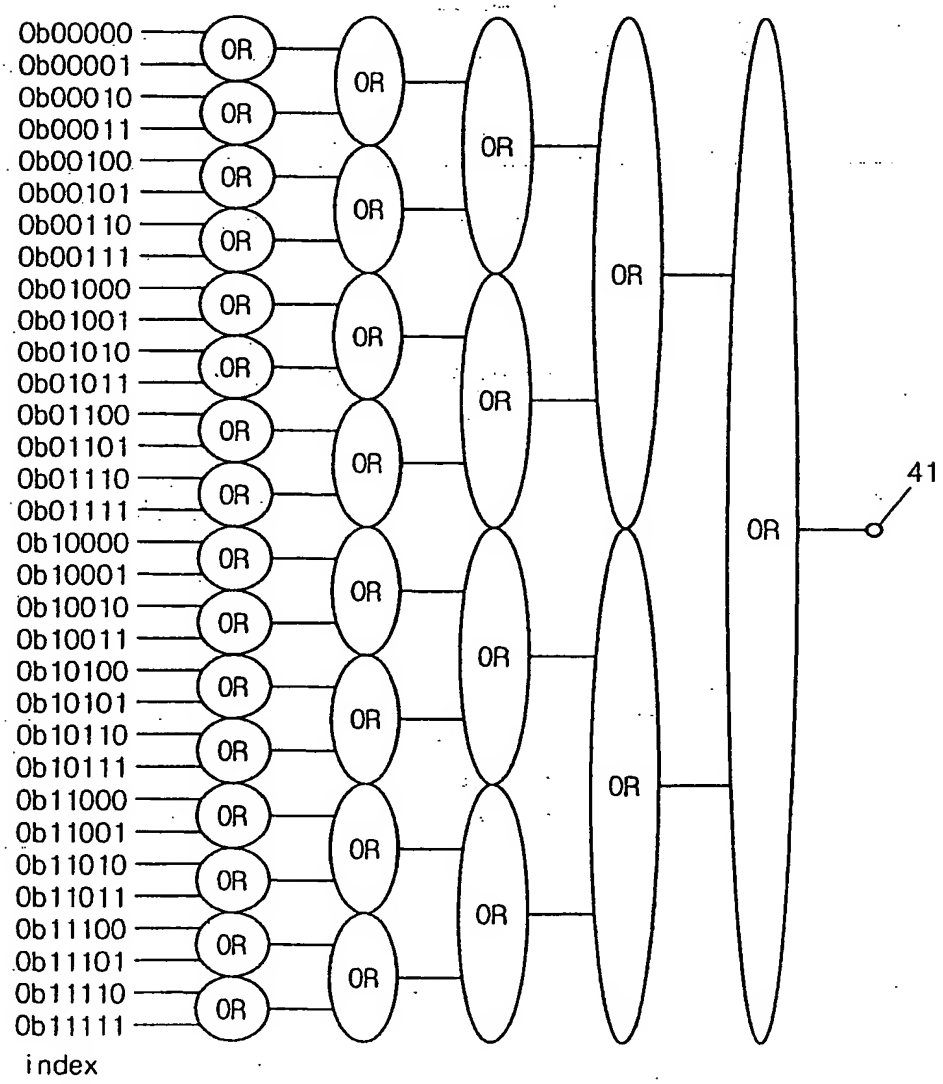

0b00000
0b00001
0b00010
0b00011
0b00100
0b00101
0b00110
0b00111
0b01000
0b01001
0b01010
0b01011
0b01100
0b01101
0b01110
0b01111
0b10000
0b10001
0b10010
0b10011
0b10100
0b10101
0b10110
0b10111
0b11000
0b11001
0b11010
0b11011
0b11100
0b11101
0b11110
0b11111
index
OR
41

FIG. 9

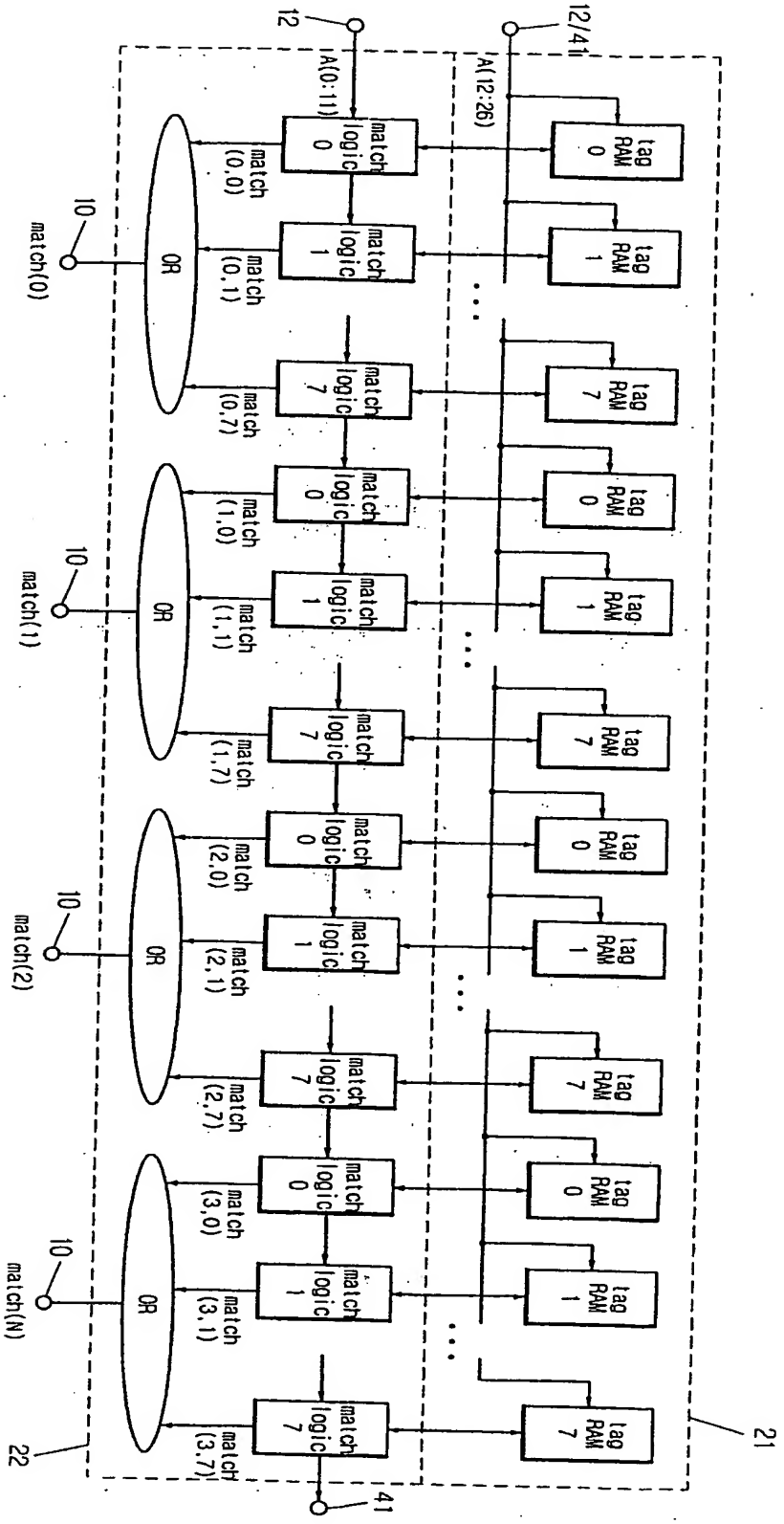

12
12/41
A(0:11)
A(12:26)
match logic 0
match logic 1
match logic 7
tag RAM 0
tag RAM 1
tag RAM 7
match (0,0)
match (0,1)
match (0,7)
match (1,0)
match (1,1)
match (1,7)
match (2,0)
match (2,1)
match (2,7)
match (3,0)
match (3,1)
match (3,7)
OR
10
match(0)
match(1)
match(2)
match(N)
21
22
41

FIG. 10

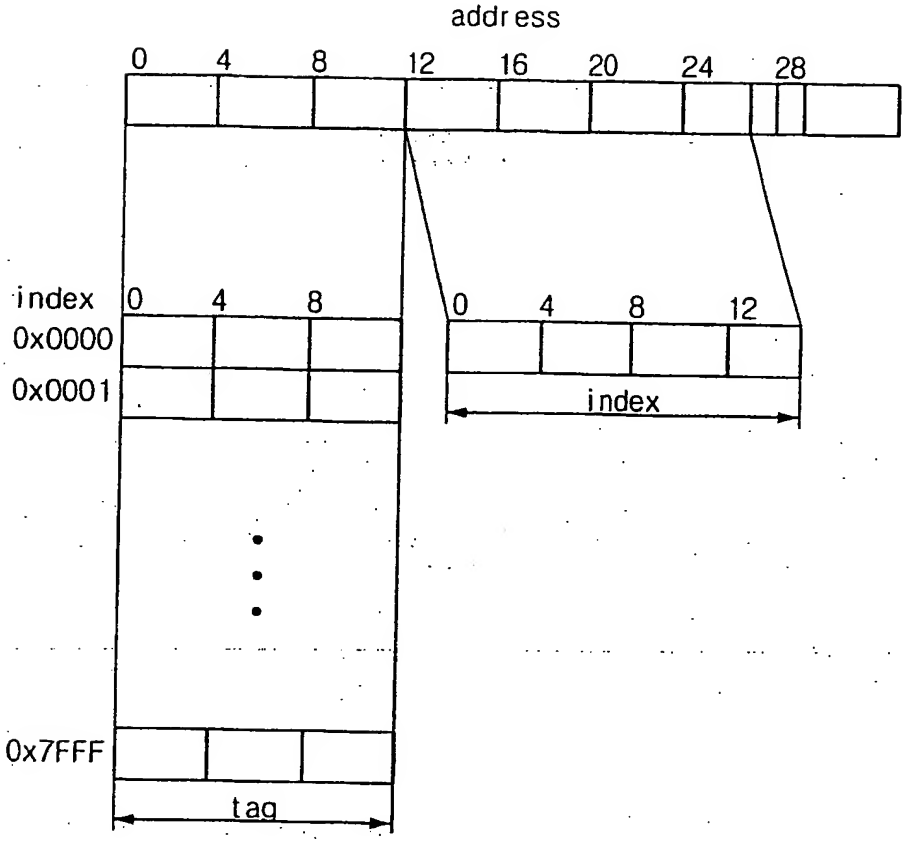

address
0
4
8
12
16
20
24
28
index
0
4
8
0
4
8
12
0x0000
0x0001
index
0x7FFF
tag

FIG. 11

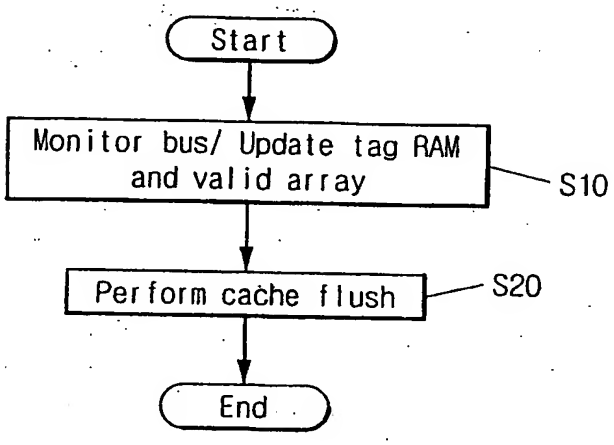

Start
Monitor bus/ Update tag RAM and valid array
S10
Perform cache flush
S20
End

FIG. 12

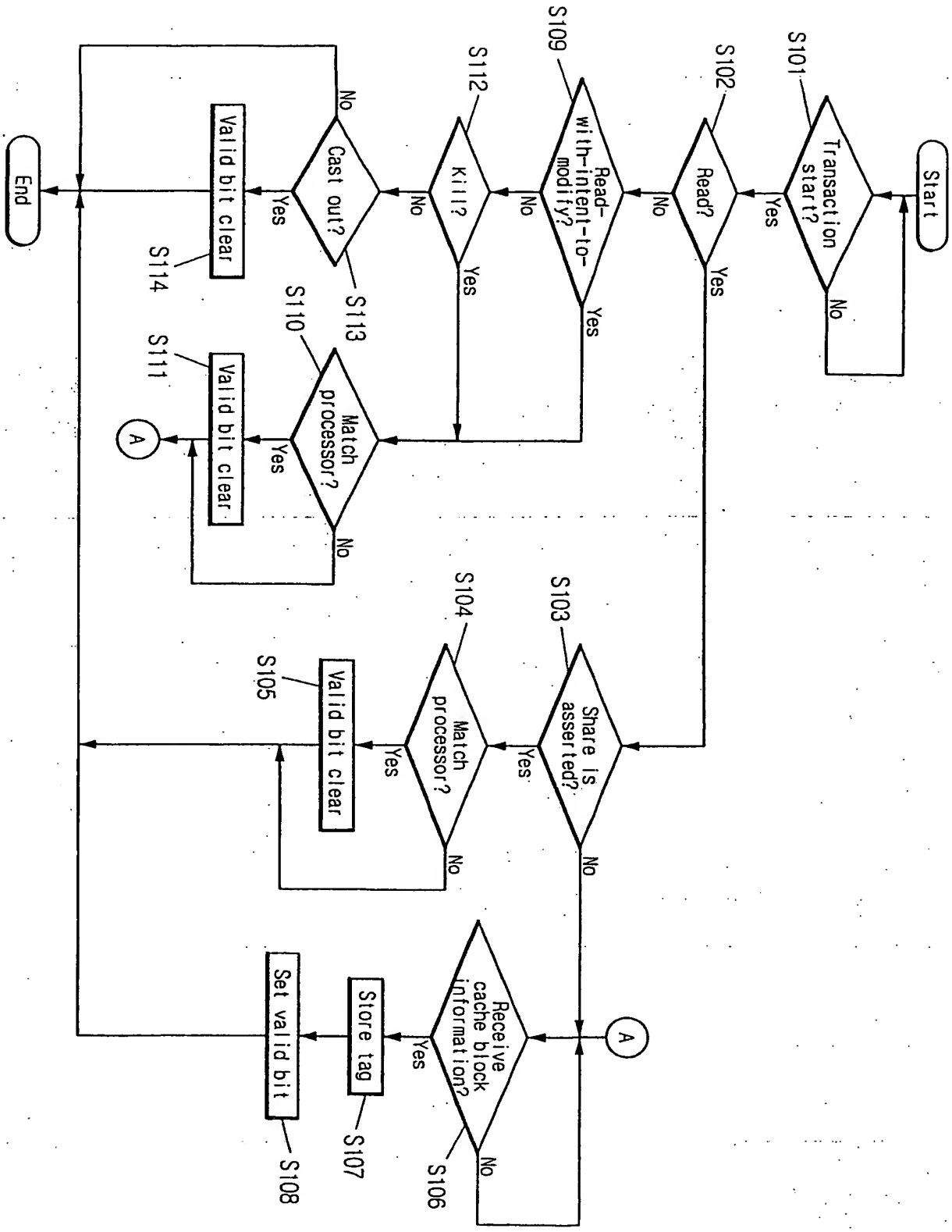

Start
Transaction start?
S101
Yes
No
Read?
S102
No
Yes
Read-with-intent-to-modify?
S109
No
Yes
Kill?
S112
No
Yes
Cast out?
S113
No
Yes
Valid bit clear
S114
End
Match processor?
S110
Yes
No
Valid bit clear
S111
A
Share is asserted?
S103
Yes
No
Match processor?
S104
Yes
No
Valid bit clear
S105
A
Receive cache block information?
S106
Yes
No
Store tag
S107
Set valid bit
S108

FIG. 13

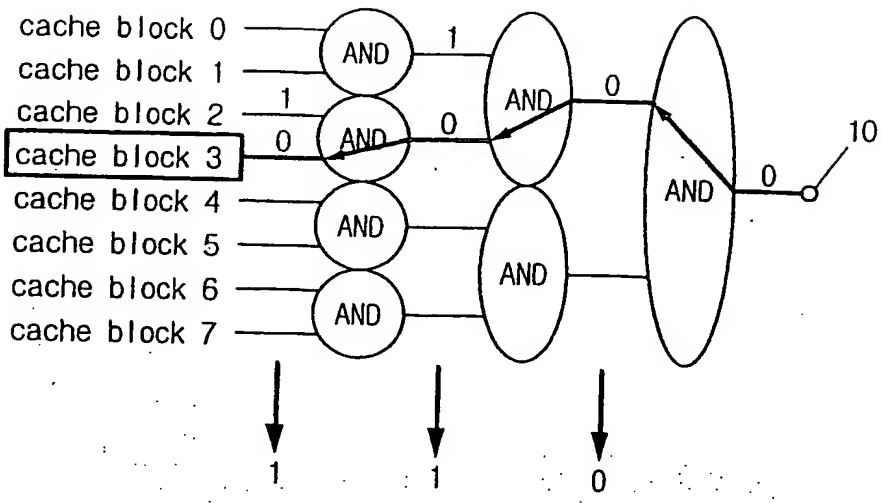

cache block 0
cache block 1
cache block 2
cache block 3
cache block 4
cache block 5
cache block 6
cache block 7
AND
AND
AND
AND
AND
AND
AND
1
1
0
1
0
0
0
10
1
1
0

FIG. 14

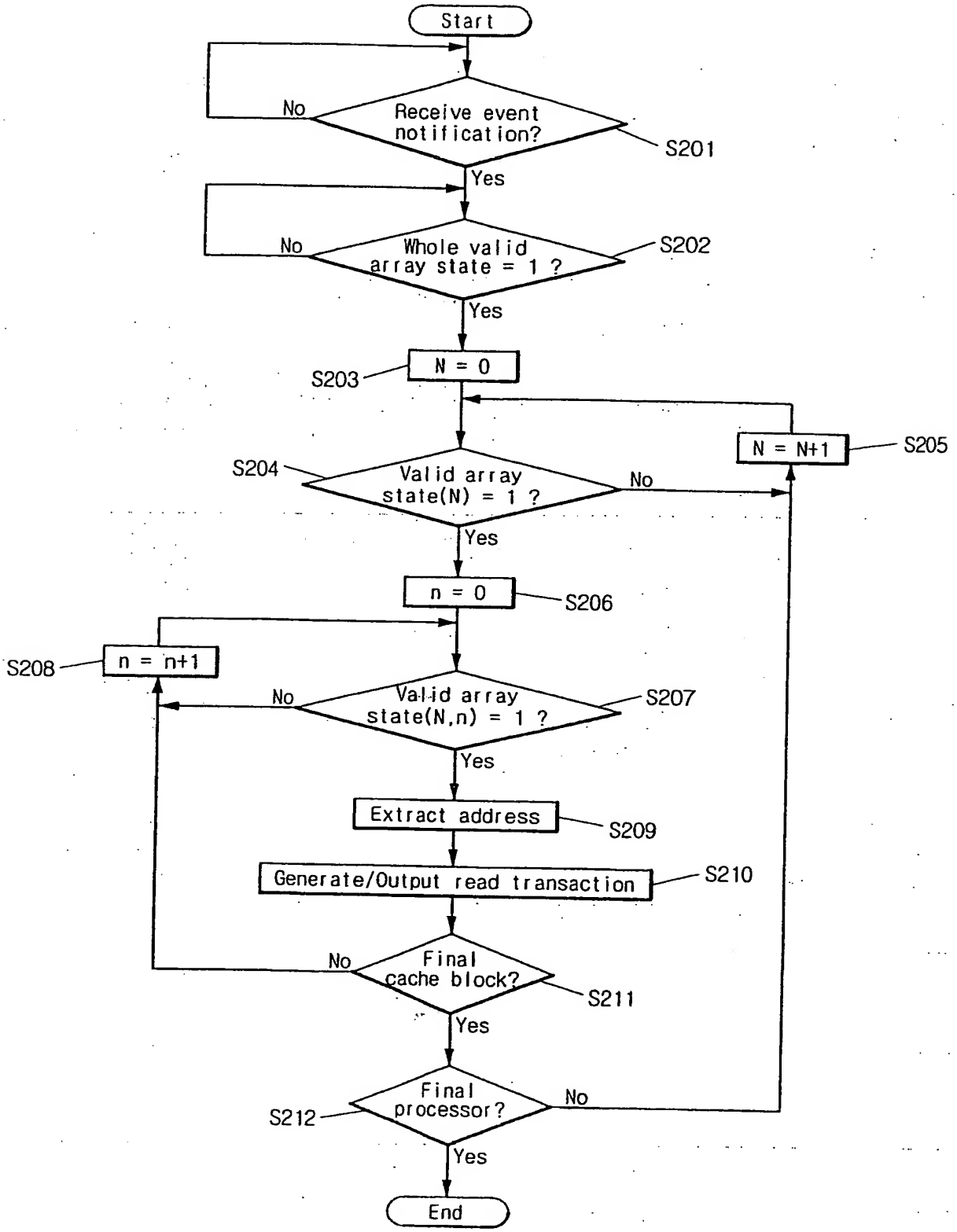
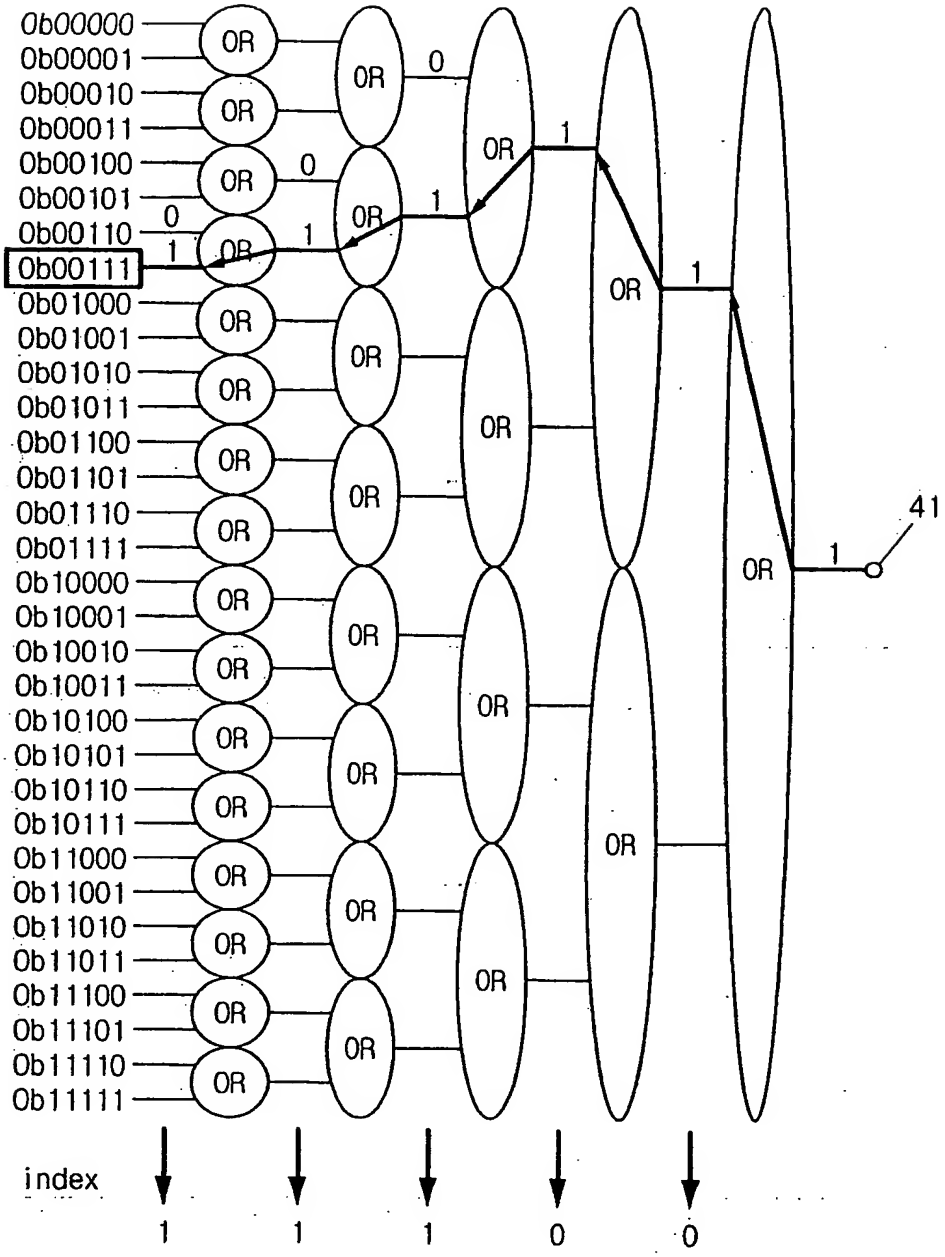

Start
Receive event notification?
No
Yes
S201
Whole valid array state = 1 ?
No
Yes
S202
N = 0
S203
Valid array state(N) = 1 ?
No
Yes
S204
N = N+1
S205
n = 0
S206
n = n+1
S208
Valid array state(N,n) = 1 ?
No
Yes
S207
Extract address
S209
Generate/Output read transaction
S210
Final cache block?
No
Yes
S211
Final processor?
No
Yes
S212
End

FIG. 15


0b00000
0b00001
0b00010
0b00011
0b00100
0b00101
0b00110
0b00111
0b01000
0b01001
0b01010
0b01011
0b01100
0b01101
0b01110
0b01111
0b10000
0b10001
0b10010
0b10011
0b10100
0b10101
0b10110
0b10111
0b11000
0b11001
0b11010
0b11011
0b11100
0b11101
0b11110
0b11111
OR
0
1
41
index
1
1
1
0
0